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GaAs MESFET - APPLICATIONS IN DIGITAL LOGIC AND COMPARATIVE ANALYSIS OF THEIR PARAMETERS

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Abstract—*The paper presents a model of GaAs (Gallium Arsenide) MESFET (Metal Semiconductor Field Effect Transistor) based digital logic using LTSPICEIV (Linear Technology simulation Program with Integrated circuit emphasis) software. We have designed a digital logic circuit of NAND gate with physical input parameters by using LTSPICEIV software and output of the same has been analyzed by this technology. MESFET based devices have better noise immunity and faster operation than any other transistor based devices. We also did a comparative analysis of Ids (Drain to Source current) w.r.t Vds (Drain to source Voltage) at various Vgs (Gate to Source Voltage). Effect on Ids by varying the Vgs has also been observed graphically by using MS-Excel. EEncouraging results are obtained from simulation of GaAs MESFET based NAND digital logic circuit while in comparative analysis of Ids w.r.t Vds it is found that Ids is maximum at Vgs with zero voltage and it goes on decreasing with more negative gate voltage.*

Keywords: *GaAs, MESFET, Simulation, Model, LTSPICEIV*

1. INTRODUCTION

With the advent of manufacturing processes which can combine many MESFETs in to an integrated circuit it is now possible to perform complex analogue filtering and signal processing at frequencies much high than Silicon devices can.

MESFET is simply a JFET fabricated in GaAs which forms a metal-semiconductor gate region known as a Schottky diode. This transistor operates like a junction-gate FET (quite similarity in construction and terminology), with a difference that it has a gate-channel Schottky(metal-semiconductor) barrier instead of a gate-channel on junction as in JFET[1]. The GaAs FET or MESFET have some common features with that of JFET, but it offers superior performance as compared to that JFET, especially in RF amplifiers. MESFETs usually make use of compound semiconductor technologies for their construction such as GaAs, InP, or SiC. They are faster but costlier than silicon-based JFETs or MOSFETs.

In 1966, the first MESFETs were developed and after one year their extremely high frequency RF microwave performance was demonstrated [2]. However, since 1984, high-speed logic circuits employing MESFETs have been produced commercially [1].

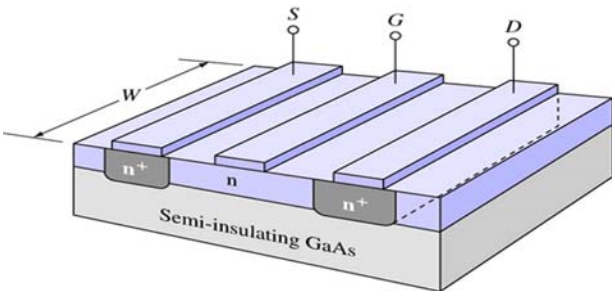

Fig. 1.1: A diagram of gallium arsenide (GaAs) MESFET (metal-semiconductor field-effect transistor) [7].

The length of this metal gate transistor is typically 0.5 to 1.0µm for discrete transistors but for ICs it can be 0.2µm [3]. As far as Gate width is concerned it is much wider than its length, typically 900 to 1200µm [3]. In this paper, Gate length is taken 0.5 µm with Gate Width 300 µm for comparative analysis.

A new model of GaAs MESFET based universal gates has been designed, analyzed, and reviewed. The schematic diagram of GaAs based NAND Gate is shown in Fig.2.1 .The structure of this circuit is designed in a simulation software i.e LTSPICE [4].

LTSPICE stands for Linear Technology Simulation Program with Integrated Circuit Emphasis. It is just a software program in which circuit description is inserted as input and output comes in the form of text data or graphical plots.

2. CALCULATIONS

For simulation of GaAs MESFET based NAND digital logic circuit, LTSPICE software is being used. The circuit design of this gate is being designed by the help of various tools in LTSPICE with physical input parameters. The circuit design is shown in fig. 2.1.

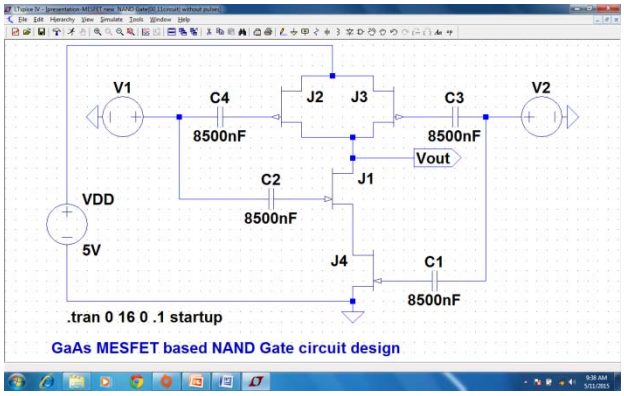

Fig. 2.1: GaAs MESFET based NAND Gate design circuit

The truth table of NAND Gate is used for observing the output of above design, which is shown in table 2.1

Table 2.1: Truth Table of NAND Gate

INPUTS		OUTPUT
Clock Pulse A	Clock Pulse B	Clock Pulse Y Y=A.B
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	HIGH
HIGH	HIGH	LOW

Now, for comparative analysis of V-I characteristic curve of GaAs based MESFET the readings [5] are as follows:

Gate Length = 0.5µm

Gate Width = 300 µm

Pinch off voltage = -0.6V

Saturation Current = 1mA

Table 2.2: Readings for V-I characteristics of GaAs based MESFET

Vds (V)	Ids (mA) Vgs = 0.0V	Ids (mA) Vgs = -0.2V	Ids (mA) Vgs = -0.4V	Ids (mA) Vgs = -0.6V
0.2	12	11	10	8
0.4	22.5	21	18.2	15.5
0.65	32	28	25.3	20.1
0.8	39	35.2	29.1	22.3
1	44	37.5	30.5	24.1
1.65	46.2	39.3	31.4	24.9
1.8	47.5	40.2	32.5	25.5
2	48	41.2	33	26
2.2	48.5	41.5	34.3	26.5
2.4	49.8	42.5	34.5	27.4
2.6	50	42.5	34.8	28
2.8	50.5	43	35	29.2
3	50.8	43.5	35.5	29.2
3.4	51	43.9	35.8	29.8
3.6	51.1	44	36	29.9

3. RESULTS

The simulation result of GaAs MESFET based NAND Gate in also shown in LTSPICE. Fig 3.1 proves the truth table of that NAND Gate (Table 2.1).

The experimental result shows that if we apply proper physical input parameters to the circuit then the output for both the low inputs will be high (Fig 3.1) and for both the high inputs it will be low (Fig. 3.1). If one input is low and other is high then output will remain high (Fig. 3.2) [4]. It follows NAND operation.

For comparative analysis of V-I characteristics of GaAs MESFET, MS-EXCEL software is being used. The output is shown in Fig.3.3. The graph is between Vds & Ids at various Vgs. It is observed that the current is maximum when Vgs is at 0V and as the value of Vgs or gate voltage goes negative, it decreases with more negative value [6].

The specifications of semiconductor based capacitor are:

Length (L): - 150 nm, Width (W): - 450 nm, Junction Bottom Capacitance:-0.2nF/m, Junction Sidewall Capacitance: -0.5nF/m, Narrowing due to side etching: -50nm [4].

With the reference of previous research paper, here we gave the application of MESFET as NAND gate [5].Here we also analyse the comparison of Vds w.r.t Ids at varying Vgs.

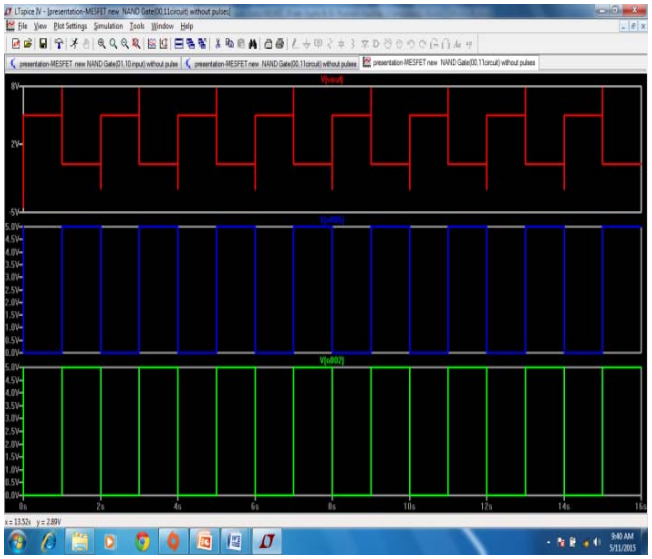

Fig. 3.1: Output waveform of GaAs MESFET based NAND Gate at 00,11 input

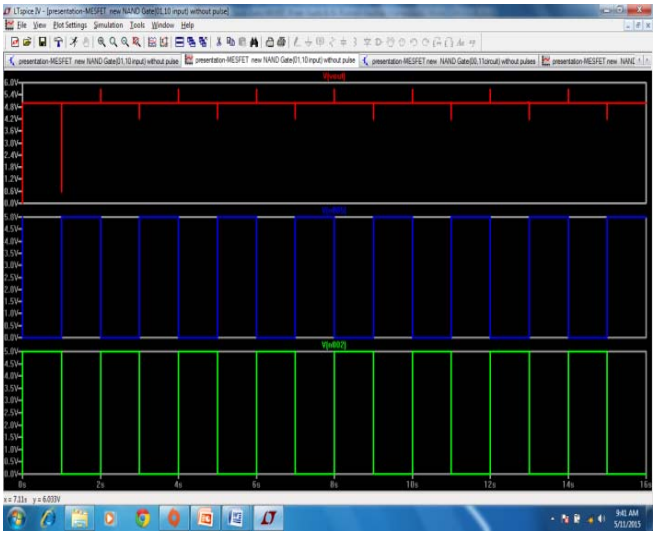

Fig. 3.2: Output waveform of GaAs MESFET based NAND Gate at 01, 10 input

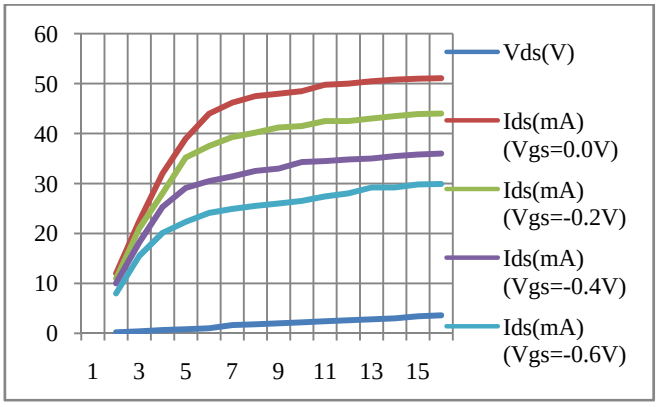

Fig. 3.3: Comparative analysis of Ids w.r.t Vds at varying Vgs.

4. CONCLUSION

From the above analysis, we have been concluded that simulation results of GaAs MESFET as a NAND Gate are satisfactory. The comparative analysis showed drain current maximum at Vgs=0V and further decrease in its value at more negative gate voltage.

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REFERENCES

[1] (http://cajstar.blogspot.in/2013/11/vlsi-technology1.html)

[2] GaAs FET MESFET radio-electronics.com.

[3] http://technology-electronic.blogspot.in/

[4] Saradindu Panda**, "**Comparative Study of Power, Delay and Noise of Logic Gates between CMOS and GaAs MESFET**"** (IJAREEIE-Vol. 1, Issue 1, July 2012)

[5] Dr.Poonam Kaushik**,**"Photolithography Processes of MESFETs and DC Characteristics"(2003),SSPL Timarpur-Delhi

[6] Mikael Andersson, "GaAs MESFET Modeling for digital Integrated circuit simulation" (January 1991).

[7] ECE3080-L-12b-AdvancedFETDevices.pdf